REMARKS

Summary of Office Action

Claims 2, 3, and 18-22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Nose et al. (US Pat. No. 6,819,311) in view of the alleged Applicant Admitted Prior Art (hereafter AAPA) of FIG. 3.

Claims 5-17 stands allowed.

Summary of Amendment

None of the claims have been amended at this time. Claims 2, 3 and 5-22 are currently pending for further consideration.

Allowed Claims

Applicants wish to thank the Examiner for allowance of claims 5-17. Based on the comments below, Applicants respectfully submit that the other pending claims (i.e., claims 2, 3, and 18-22) are also in condition for allowance.

All Claims Comply With §103

Claims 2, 3, and 18-22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Nose et al. (US Pat. No. 6,819,311) in view of the alleged Applicant Admitted Prior Art (hereafter AAPA) of FIG. 3. Applicants respectfully traverse these rejections.

As stated in the previous response (filed 9/29/2005) and incorporated herein by reference, independent claims 2 and 3 recite, in part, the step of "applying first to third gate output enable signals to the gate driver." Claim 18 recites, in part, the step of "selecting two gate lines that are separated by a predetermined number of gate lines based on received first to third gate output

enable signals." Nose et al. teaches applying ***one*** output enable signal (OE) that are applied simultaneously to all the gate drivers. Nose et al. uses pairs of inverters (FIGs. 11, 15, 18, 19) to alternately select which gate drivers are enabled. As stated previously, Nose et al. does not teach or suggest at least the steps indicated above for claims 2, 3, and 18. The Office Action refers to FIG. 3 of the present application as allegedly teaching the "missing" feature. Applicants disagree.

FIG. 3 of the present application illustrates the relationship of the gate output enable signal (GOE) and the gate lines used in conventional gate driving circuits. As explained on page 3, paragraph [0006]-[0007], FIG. 3 is a representation of the GOE and gate driver relationship with respect to the driving waveform as shown in FIG. 2. Therefore, FIG. 3 needs to be viewed in context with the teachings of FIG. 2. FIG. 2 illustrates the timing and waveform diagram of known circuits. As shown in FIG. 2, the each of the GOE1-GOE3 signals is sequentially applied in sequential time periods (i.e., one GOE signal in one time period) to sequentially select one gate line in sequential order. There is no explanation or rationale as to why one with ordinary skill in the art would apply three GOE signals to a circuit of Nose et al. that is specifically designed to operate on only one OE signal.

Nose et al. teaches a circuit that is designed and adapted to select two gate lines in one time period using only one OE signal. The related art of FIG. 3 (in context with FIG. 2) discloses a method of sequentially selecting one gate line per time period using three GOE signals. There is no suggestion or teaching to make obvious to one of ordinary skill in the art to modify Nose et al. to use three GOE signals. Rather, applying three GOE signals to the circuit in

Nose et al. would render the circuit inoperable as the selection of the two gate lines are an operation of the inverse (via the inverters) of the applied OE signal. Because Nose et al. teaches a completely different method of driving the LCD display than that of the related art of FIG. 3, it would not have been obvious for one with ordinary skill in the art to have incorporated the application of three GOE signals to the circuit of Nose et al. that uses only one OE signal.

The Office asserts that one with ordinary skill in the art would have been motivated to incorporate the applying of first to third gate output enable signals to the gate driver as taught by AAPA in the system of Nose "in order to prevent a crosstalk phenomenon between pixel of displays." It is noted that the circuit of Nose et al. already prevents crosstalk phenomenon because the selected pixels are separated by a black display selection period (see FIG. 2 of Nose et al.). Hence, Applicants respectfully assert that one with ordinary skill ***would not have been motivated*** to apply three GOE signals (AAPA: FIG. 3) to the circuit of Nose et al. since doing so would render the circuit of Nose et al. inoperable in order to solve a problem (i.e., crosstalk phenomenon) that does not exist in Nose et al.

Additionally, claim 18 recites, in part, the step of "***selecting two gate lines*** that are separated by a predetermined number of gate lines ***based on received first to third gate output enable signals***." (Emphasis added.) Nose et al. and the related art FIG. 3 both fail to teach or suggest such a feature. Accordingly, Applicants respectfully request that the rejection to claims 2, 3, and 18-22 be withdrawn.

CONCLUSION

In view of the foregoing, reconsideration and timely allowance of the pending claims are respectfully requested. Should the Examiner feel that there are any issues outstanding after consideration of the response, the Examiner is invited to contact the Applicants' undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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